REMARKS

No new matter has been added to the specification. The specification has been revised to more accurately define the invention disclosed in the patent application as filed on June 30, 2000.

The new FIG. 3 submitted herewith accurately depicts the disclosure of the invention set forth in the specification. FIG. 3 has been revised to accurately reflect the description number for the display memory 222 and video decoder 230. The revision to the description number is in red. No new matter is included in new FIG. 3. Therefore, Applicants request that FIG. 3 attached hereto be included with the above referenced patent application and replace FIG. 3 as filed on June 30, 2000.

The new FIG. 4 submitted herewith accurately depicts the disclosure of the invention set forth in the specification. FIG. 4 has been revised to delete comments to the inventors for their review of the figure. The deleted language is notated with red hash marks. No new matter is included in new FIG. 4. Therefore, Applicants request that FIG. 4 attached hereto be included with the above referenced patent application and replace FIG. 4 as filed on June 30, 2000

Respectfully submitted,

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: U.S. Patent and Trademark Office, Washington, DC 20231 on July 18, 2001.

Marilyn Bass July 18, 2001

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE DRAWINGS

FIG. 3 has been amended as follows:

Please delete "240" as the description number for VIDEO DECODER and replace with – 230 -- ;

Please delete "230" as the description number for DISPLAY MEMORY and replace with – 222 --.

FIG. 4 has been amended as follows:

Please delete the word "Optional" and the line extending therefrom;

Please delete the words "Where is our invention used in one of the embodiments" and the line extending therefrom.

IN THE SPECIFICATION

The paragraph beginning on page 6, line 25, has been amended as follows:

Display controller 220 is also provided with a display memory ~~230~~ 222, which stores pixel data in text, graphics, or video modes for output to display 290. Host CPU 210 is be coupled to display controller 220 through bus 270 and updates the content of display memory ~~230~~ 222 when a display image for display 290 is altered. Bus 270 may comprise, for example, a PCI bus or the like. System memory 280 may be coupled to Host CPU 210 for storing data. Hardware video decoder ~~240~~ 230 is provided to decode video data such as, for example, MPEG video data. MPEG video data is received from an MPEG video data source (e.g., CD-ROM or the like). Alternatively, the video decoder ~~240~~ 230 is implemented as, for example, a ~~convention~~ conventional software decoder 282 stored in the system memory 280. As such, one of ordinary skill in the art will recognize that the teaching of the present invention may be implemented in either software or hardware video decoders. Once decoded, the decoded video data is outputted to system memory 270 or directly to display memory 230.

The paragraph beginning on page 7, line 11, has been amended as follows:

Referring to FIG. 4, the components of ~~the~~ a video decoder 240 according to a first embodiment of present invention are further described. The video decoder 240 may be utilized as the hardware decoder 230 or software decoder 282 within the computer system 200. MPEG data received from an MPEG data source may be decoded and decompressed as follows. The video decoder 240 receives an MPEG bit stream 242 at a Variable Length Decoding (VLD) block 244. The VLD block 244 decodes the MPEG bit stream 242 and generates a quanitized block 246 that is transferred to an Inverse Quantanization Block (IQ block) 266. The IQ block 266 performs inverse

quantization on the quantized block 246 to generate a frequency spectrum 268 for the quantized block. An Inverse Discrete Cosine Transform (IDCT) block 246~~.~~ performs inverse discrete cosine transformation of the quantized block 246 using the frequency spectrum 268 to generate a decoded block 252 ~~in YUV planar format~~ that is transferred to the motion compensation block (MCB) 248. Motion compensation is performed by the MCB 248 to recreate the MPEG data 256 ~~in YUV planar format. Color~~ Finally, color conversion block 262 converts the MPEG data 256 ~~from YUV color space format to~~ into the Red, Green, Blue (RGB) color space in order to generate pictures 264.

The paragraph beginning on page 7, line 25, has been amended as follows:

Conventional MPEG decoders, such hardware video decoder ~~240~~ 230 or software video decoder 282, decode a compressed MPEG bit stream into a storage format depending on the particular compression format used to encode the MPEG bit stream. For the reasons described above, YUV planar format is the preferred format for compression of MPEG images within conventional MPEG decoders. Consequently, the decoded block 252 outputted by the IDCT block 250 as well as the MPEG data 256 outputted by the MCB 254 are generated in YUV planar format within conventional MPEG decoders. Unfortunately, YUV planar format is an inefficient format during motion compensation of the decoded block 252.

The paragraph beginning on page 8, line 6, has been amended as follows:

Accordingly, FIG. 5C depicts ~~the~~ a novel mixed storage format 300 described by the present invention that is utilized by the video decoder 240. Careful review of FIGS. 5A-5C illustrates that Y component values are stored in a planar array 300A while the U and V components are interleaved in a packed array 300B. Using the mixed storage format 300, decoded block 252 received from the IDCT block 246 is converted from planar format (FIG. 5B) to the mixed storage format 300. Storage of reference frames 260 and MPEG data 256 in the mixed storage format 300 optimizes motion compensation of the decoded block 252 as depicted in FIGS. 6A and 6B.